28 November 2025

Notification for Recruitment of Senior Research Fellow, Electrical Engineering
Project funded by the MeitY Chips to Startups (C2S)
Ref: IITPKD/2025/045/EE/SUM

- **Project Areas:** ASIC/ FPGA based system design for real-time signal processing and machine learning applications in the domain of ultra wideband (UWB) radar design. Work will involve algorithm design, optimization, VLSI architecture design, Verilog coding, verification, debugging, and finally ASIC/FPGA prototyping.
- **Required Skills:**
  - Strong digital design skills using Verilog, ASIC design flow using EDA tools, Vivado FPGA design flow
  - Good knowledge and understanding of MATLAB/ Python for algorithmic study.
- **Eligibility:**
  - B. Tech. in Electronics and Communication Engineering with at least 65% marks.
  - M. Tech. in Signal Processing or VLSI Design
  - At least 3 years' research experience in Digital VLSI Design.
- **Age:** Candidates who are not exceeding 35 years of age, as on the closing date of application, with relaxation to candidates belonging to OBC/ SC/ ST/ PWD categories and women applicants as per Government of India norms.
- **Appointment Duration:** 12 Months
- **No. of Positions:** One
- **Salary Particulars:** The monthly remuneration for this position will be Rs. 42,000/- (Forty-Two Thousand Rupees Only). Hostel accommodation may be provided at the institute based on availability on a chargeable basis. In case of non-availability of institute hostel, admissible HRA will be provided as per the Government of India rules.
- **Deadline for application**: 05 December 2025 (Friday)

Candidates satisfying the required skills may send their resumes and certificates pertaining to educational qualifications starting from class X (in a single PDF) to "**svmula@iitpkd.ac.in**". The subject of the application e-mail should be "Application for Senior Research Fellow - **IITPKD/2025/045/EE/SUM**". The candidate is expected to join immediately after receiving the offer letter.

****