Indian Institute of Technology Palakkad
भारतीय प्रौद्योगिकी संस्थान पालक्काड
Under Ministry of Education, Govt. of India
शिक्षा मंत्रालय के अधीन, भारत सरकार

IIT PALAKKAD

15 April 2021

Notification for Recruitment of Junior Research Fellow – Electrical Engineering

Project funded by SERB Start-up Research Grant

Ref: IITPKD/2021/014/EE/SUM

- **Project areas:** VLSI Architectures for real-time signal processing applications. The scope of the project is to design and implement real-time adaptive filtering algorithms on an FPGA platform. Work will involve algorithm design, VLSI implementation and FPGA prototyping.
- **Required skills:** The candidate should have good knowledge and understanding of MATLAB/ Python, Verilog, Vivado Design Flow and FPGA prototyping.
- **Eligibility:** B.E./ B.Tech with valid GATE score or M.E./M.Tech (VLSI design / Signal Processing or allied areas) from reputed institutions
- **Appointment duration:** Initially for six months with the possibility of extension depending on satisfactory performance of the candidate and availability of funds
- **No. of Positions:** One
- **Salary Particulars:** The monthly remuneration for this position will be Rs. 31,000/- (Thirty One Thousand Rupees Only). Hostel accommodation may be provided at the institute based on availability on a chargeable basis. In case of non-availability of institute hostel, admissible HRA at 8% will be provided as per Government of India rules.
- **Deadline for application**: 01 May 2021 (Saturday)

Candidates satisfying the required skills may send their resumes to "**svmula@iitpkd.ac.in**". The subject of the application e-mail should be **Application for Junior Research Fellow - IITPKD/2021/014/EE/SUM.**

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