IIT PALAKKAD

Sandeep Chandran

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Research Interests

- Computer Architecture and High-performance computing
- Post-silicon Validation and Runtime Verification

Brief Summary of Research

Sandeep investigates design and verification challenges when scaling high-performance systems. On the design front, his research focuses on using a combination of modern architectures where there is a reconfigurable fabric alongside a processor, and system-level modifications to increase single-thread performance beyond state-of-the-art processors. On the verification front, he focuses on finding ways to make post-silicon validation techniques efficient and privacy-aware so that teams from across companies can collaborate without compromising their Intellectual Properties (IPs). Prior to joining IIT Palakkad, he was part of the performance modelling team at AMD India Private Limited. He has published papers in top-tier journals and conferences, and has offered his services by performing peer-reviews, and as a member of the Technical Program Committee for ACM/IEEE Conferences.

Projects

- Institute Grant to setup Advanced Architecture Lab at IIT Palakkad (INR 28.99 lakhs)

Recent Publications

- Neetu Jindal, **Sandeep Chandran**, Preeti Ranjan Panda, Sanjiva Prasad, Abhay Mitra, Kunal Singhal, Shubham Gupta, and Shikhar Tuli, "*DHOOM: Reusing Design-for-Debug Hardware for Online Monitoring"* in ACM/IEEE DAC'19, Las Vegas, USA, 2019
- Invited Book Chapter titled "*Debug Data Reduction Techniques"* by **Sandeep Chandran**, and Preeti Ranjan Panda, in Post-silicon Validation and Debug, SPRINGER 2018