**Satyajit Das**
Ph.D. University of South Brittany, France, and University of Bologna, Italy
Assistant Professor, Computer Science and Engineering
satyajitdas@iitpkd.ac.in
https://iitpkd.ac.in/people/satyajitdas

## Research Interests

- Coarse Grained Reconfigurable Array (CGRA)
- Heterogeneous Multi-Core System on Chip (SoC)
- Low Power Design
- Reconfigurable Computing
- High Level Synthesis
- Digital Architecture
- Cryptography

## Brief Summary of Research

My research spans the areas of architecture, methods, and tools for embedded systems, including CGRAs, custom processors, multi-cores, high-level synthesis, and compilers. The focus of my research is to implement highly energy efficient solutions for digital architectures in the domain of heterogeneous and reconfigurable multi-core System on Chips (SoCs). This includes architectures, design implementation strategies, runtime, and compilation support. He has published several research papers in refereed international journals including IEEE TCAD, IJNS and conferences including ASPDAC, DATE, ISVLSI, ISCAS. He is currently a member of the advisory committee of a Ph.D. student in University of South Brittany, France collaborated with University of Bologna, Italy.

## Recent Publications

- S. Das, D. Rossi, K. Martin, D. Rossi, P. Coussy, L. Benini,"An Energy-Efficient Integrated Programmable Array Accelerator and Compilation flow for Near-Sensor Ultra-low Power Processing," in **IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems**. doi: 10.1109/TCAD.2018.2834397
- S. Das, K. Martin, P. Coussy, “Context-memory Aware Mapping for Energy Efficient Acceleration with CGRAs”, In 2019 **Design, Automation & Test in Europe Conference & Exhibition (DATE)** (pp. 336-341). IEEE.
- S. Das, K. Martin, P. Coussy, D. Rossi, “A Heterogeneous Cluster with Reconfigurable Accelerator for Energy Efficient Near-Sensor Data Analytics”, In Proceedings of **IEEE International Symposium on Circuits and Systems (ISCAS)**, Florence, IT, 2018 pp. 1-5
- **S. Das**, K. Martin, D. Rossi, P. Coussy, L. Benini, “Efficient Mapping of CDFG onto Coarse Grained Reconfigurable Array Architectures”, In proceedings of 22nd **Asia and South Pacific Design Automation Conference (ASP-DAC)**, Tokyo, Japan, 2017, pp.127-132